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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/555,096	11/02/2005	Yoshiyuki Kajiwara	280664US6PCT	9435

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EXAMINER	
VLAHOS, SOPHIA	
ART UNIT	**PAPER NUMBER**
2611	

NOTIFICATION DATE	DELIVERY MODE
03/02/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/555,096	KAJIWARA, YOSHIYUKI	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/02/05, 11/04/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority (JAPAN 2004-112318 filing date 04/06/2004) under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 11/02/2005 and 11/04/2008 have been considered by the examiner.

Specification

3. The incorporation of essential material in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. ¶0002 of Patent Application Publication of the instant application states: “The present invention contains subject matter related to Japanese Patent Application JP2004-112318 filed in the Japanese Patent Office on Apr. 6, 2004, the entire continents of which are incorporated herein by reference.” According to 37 CFR 1.57(b) Applicant is required to “Supply an English language translation of any prior-filed application that is in a language other than English”. (Therefore an English language translation of the JP2004-112318 is required if Applicant intends to incorporate by reference the entire contents of the foreign priority patent)

Applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other

requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing the applicant, stating that the material being inserted is the material previously incorporated by reference and that the amendment contains no new matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vis (U.S. 7,012,772) in view of Fermo et al. "Simplified Volterra Filters for Acoustic Echo Cancellation in GSM receivers", September 2000 and N.B. Jones et al. "Digital Signal Processing", IEE Control Engineering Series 42, 1990, page 86 (source http://books.google.com/).

With respect to claim 5, Vis discloses: a linear section of the second-order Volterra filter for implementing a linear term of said second-order Volterra filter and for linear equalization of said input signal (Fig. 3, block 12 implements the linear term of a second order Volterra filter, column 4, lines 54-64); a quadratic section of the second-order Volterra filter for implementing a quadratic term of said second-order Volterra filter and for non-linear equalization of said input signal (Fig. 3, block 18 is the second order equalizing function block of the Volterra filter); signal summing means for summing a

signal output from said linear section and a signal output from said quadratic section together (Fig. 3, adder 34, column 4, lines 60-64); and most likelihood decoding means for most likelihood decoding a signal output from said signal summing means (Fig. 3, combination of blocks 28, 30, 20, column 5, lines 6-21);

Vis does not expressly disclose: said quadratic section including multiplication means for multiplying a first input signal and a second input signal together; said multiplication means including one or more series-connected delaying means for delaying signals output from said multiplication means each by a preset unit time, coefficient multiplying means for multiplying a signal output from said multiplication means and a signal output from each of said delaying means, each with a preset coefficient, and summing means for summing outputs of said coefficient multiplying means together.

In the same field of endeavor, (systems using Volterra filters), Fermo et al. disclose: a quadratic (Volterra filter) section including multiplication means (for multiplying a first input signal and a second input signal together (page 2, Fig. 3, simplified second order (quadratic) Volterra filter, the multiplication means comprises the top row of components to the left of adder which outputs signal y(n), see left column on same page for more details).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Vis based on Fermo et al so that a simplified Volterrra filter which approximates a second order filter is used, resulting in high computational resource savings (Fermo, page 2, first paragraph on left column).

Fermo et al. only discloses FIR filters receiving the output of the multipliers of the Volterra filter, therefore Fermo et al. do not expressly disclose: said multiplication means including one or more series-connected delaying means for delaying signals output from said multiplication means each by a preset unit time, coefficient multiplying means for multiplying a signal output from said multiplication means and a signal output from each of said delaying means, each with a preset coefficient, and summing means for summing outputs of said coefficient multiplying means together.

In the field of digital filter design, Jones et al. discloses: an FIR filter comprising: one or more series-connected delaying means for delaying input signals each by a preset unit time (page 86, Fig. 7.5 each of the "z-1" blocks is a delay unit); coefficient multiplying means for multiplying an input signal and a signal output from each of said delaying means (multiplication of the input signal xk by ao and multiplication of the delayed signal xk-1 by a1, to implement equation 7.9), each with a preset coefficient, and summing means for summing outputs of said coefficient multiplying means together (Fig. 7.5 summing block).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Vis and Fermo based on Jones et al. so that stable FIR filters (page 86 of Jones et al.) are used to implement the quadratic section of the second order Volterra filter of Vis.

With respect to claim 6, the system obtained by modifying Vis based on Fermo and Jones further includes: wherein said quadratic section includes a plurality of said

multiplication means (Fig. 3 of Fermo et al. each of the plurality of multiplication means includes a mixer, and FIR filter (having components disclosed by Jones et al.)), one of said multiplication means employing a signal not delayed from said first signal, as said second signal (Fig. 3 of Fermo, the "top" row of parallel branches, does not use a delay unit, and multiplies the input signal with itself in its respective mixer), the remaining ones of said multiplication means each employing a signal delayed a preset time from said first signal, as said second signal (Fermo, see rest of branches each having a delay unit, delaying the input signal and multiply the undelayed input signal with the respectively delayed signal).

With respect to claim 7, the system obtained by modifying Vis based on Fermo and Jones further includes: wherein said quadratic section includes n of said multiplication means, n being an integer not less than unity (Fig. 3 of Fermo et al. shows 4 multiplication means); a k'th one of said multiplication means, k being an integer such that $1 \leq k \leq n$, employing a signal corresponding to said first signal delayed by (k-1) times of said unit time, as said second signal (Fig. 3 of Fermo where n=4, and as an example k=2 (corresponding to the second multiplication means), which multiplies the undelayed received signal with a second signal delayed by 2-1=1 delay unit).

With respect to claim 8, the system obtained by modifying Vis based on Fermo and Jones further comprises: error detection means for detecting an error between a signal at each discrete time output from said signal summing means and a target signal

(Vis, Fig. 3 and Fig. 4, LMS adaptation circuit receives error signal e_k, derived from the summed signal at 34, and target signal from slicer 30, column 5, lines 5-23); said coefficient multiplying means updating said preset coefficient every discrete time based on an error detected by said error detection means (column 4, lines 51-64).

With respect to claim 9 method claim 9 is rejected based on a rationale similar to the one used to reject apparatus claim 5 above.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fermo et al. "Simplified Volterra Filters for Acoustic Echo Cancellation in GSM receivers", September 2000 and N.B. Jones et al. "Digital Signal Processing", IEE Control Engineering Series 42, 1990, page 86 (source http://books.google.com/).

With respect to claim 1, Fermo et al. disclose: a quadratic section of a second-order Volterra filter for implementing a quadratic term of said second-order Volterra filter includes multiplication means for multiplying a first input signal with a second input signal (page 2, Fig. 3, simplified second order (quadratic) Volterra filter, the multiplication means comprises the top row of components to the left of adder which outputs signal y(n), see left column on same page for more details, the multiplication means includes a mixer to multiply an input signal with a second signal).

Fermo et al. only discloses FIR filters receiving the output of the multipliers of the Volterra filter, therefore Fermo et al. do not expressly disclose: said multiplication means including one or more series-connected delaying means for delaying signals

output from said multiplication means each by a preset unit time, coefficient multiplying means for multiplying a signal output from said multiplication means and a signal output from each of said delaying means, each with a preset coefficient, and summing means for summing outputs of said coefficient multiplying means together.

In the field of digital filter design, Jones et al. discloses: an FIR filter comprising: one or more series-connected delaying means for delaying input signals each by a preset unit time (page 86, Fig. 7.5 each of the "z-1" blocks is a delay unit); coefficient multiplying means for multiplying an input signal and a signal output from each of said delaying means (multiplication of the input signal xk by ao and multiplication of the delayed signal xk-1 by a1, to implement equation 7.9), each with a preset coefficient, and summing means for summing outputs of said coefficient multiplying means together (Fig. 7.5 summing block).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Fermo based on Jones et al. so that stable FIR filters (page 86 of Jones et al.) are used to implement the quadratic section of the second order Volterra filter.

With respect to claim 2, the system obtained by modifying Fermo based on Jones further includes: wherein said quadratic section includes a plurality of said multiplication means (Fig. 3 of Fermo et al. each of the plurality of multiplication means includes a mixer, and FIR filter (having components disclosed by Jones et al.)), one of said multiplication means employing a signal not delayed from said first signal, as said

second signal (Fig. 3 of Fermo, the “top” row of parallel branches, does not use a delay unit, and multiplies the input signal with itself in its respective mixer), the remaining ones of said multiplication means each employing a signal delayed a preset time from said first signal, as said second signal (Fermo, see rest of branches each having a delay unit, delaying the input signal and multiply the undelayed input signal with the respectively delayed signal).

With respect to claim 3, the system obtained by modifying Fermo based onJones further includes: wherein said quadratic section includes n of said multiplication means, n being an integer not less than unity (Fig. 3 of Fermo et al. shows 4 multiplication means); a k'th one of said multiplication means, k being an integer such that $1 \leq k \leq n$, employing a signal corresponding to said first signal delayed by (k-1) times of said unit time, as said second signal (Fig. 3 of Fermo where n=4, and as an example k=2 (corresponding to the second multiplication means), which multiplies the undelayed received signal with a second signal delayed by 2-1=1 delay unit).

Method claim 4 is rejected based on a rationale similar to the one used to reject apparatus claim 1 above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al. (U.S. 5,471,504)

DeGroat et al. (U.S. 6,449,110)

Agarossi et al. (U.S. 6,600,794)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SOPHIA VLAHOS/
Examiner, Art Unit 2611
2/26/2009

/Mohammad H Ghayour/
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